

	L #	Hits	Search Text	DBs	Time Stamp
1	L2	69	(minimiz\$3 or reduc\$3 or eliminat\$3) near2 harmonic near2 interference	USPAT; EPO; JPO; DERWENT	2002/09/19 17:05
2	L3	21	2 and counter	USPAT; EPO; JPO; DERWENT	2002/09/19 17:11
3	L4	48	2 not 3	USPAT; EPO; JPO; DERWENT	2002/09/19 17:11
4	L5	1	4 and count\$3	USPAT; EPO; JPO; DERWENT	2002/09/19 17:13
5	L6	403 6	(clock or oscillator) and counter and ((controller or control\$3) same duty adj cycle)	USPAT; EPO; JPO; DERWENT	2002/09/19 17:14
6	L7	367	6 and harmonic	USPAT; EPO; JPO; DERWENT	2002/09/19 17:15
7	L8	0	7 and (asymetric\$3 or non adj asymmetric\$3 or nonasymmetric\$3) adj duty	USPAT; EPO; JPO; DERWENT	2002/09/19 17:16
8	L9	35	7 and 327/\$.ccls.	USPAT; EPO; JPO; DERWENT	2002/09/19 17:35
9	L10	143	7 not "35"	USPAT; EPO; JPO; DERWENT	2002/09/19 17:35
10	L11	224	7 not 10	USPAT; EPO; JPO; DERWENT	2002/09/19 17:36
11	L12	1	11 and (asymmetric\$2 or non adj symmetri\$2 or non-asymmetri\$2) adj duty	USPAT; EPO; JPO; DERWENT	2002/09/19 17:39
12	L13	223	11 not 12	USPAT; EPO; JPO; DERWENT	2002/09/19 17:50
13	L14	35	(327/\$.ccls. or 331/\$.ccls.) and (oscillator or clock) and counter and (low adj frequency same duty adj cycle)	USPAT; EPO; JPO; DERWENT	2002/09/19 17:52

ABSTRACT

Systems and methods are disclosed for minimizing nth-order harmonic associated with a square wave clock signal having a predetermined frequency and a duty cycle. The system changes the duty cycle of the clock to eliminate or suppress the nth-order harmonic of the clock; and generates a low-interference clock having the changed duty cycle while keeping the predetermined frequency.

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